Notice of Allowability	Application No. 10/740,033	Applicant(s) CERNY ET AL.	
	Examiner Phallaka Kik	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Application filed on 12/18/2003 and interview conducted on 1/20/2006 and 2/8/2006*.

2. ☒ The allowed claim(s) is/are *2,5,7-19,21,23, wherein claims 1,3-4,6,20,22 have been canceled and claims 2,5,7-19,21,23 have been renumbered as 1-17, respectively*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20060202* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This Office Action responds to the Application filed on 12/18/2003 and interview conducted on 1/20/2006 and 2/8/2006. Claims 1-23 are pending, wherein claims 1,3-4,20,22 are withdrawn from consideration as being directed to non-elected invention with traverse as given below. Claims 2,5,7-19,21,23 have been examined and are allowed, wherein claims 1-4,7,20-22 are subjected to the following Examiner's Amendment.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1,3-4,6,20,22 drawn to electromagnetic waveform/method/computer program for performing formal verification of a representation of an electronic design of an IC involving the formal verification step, classified in class 716, subclass 5.

II. Claims 2,5,7-19,21,23, drawn to electromagnetic waveform/method/computer program for performing simulation verification involving conversion steps, classified in class 716, subclass 3.

3. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as performing the formal verification step/process on circuit representation produced by other methods/systems other that of invention II. See MPEP § 806.05(d).

4. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Johnathan T. Kaplan (Reg. No. 38,935) on 1/20/2006 a provisional election was made with traverse to prosecute the invention of group II, claims 2,5,7-19,21,23. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1,3-4,6,20,22 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Since this application is in condition for allowance except for the presence of claims 1,3-4,6,20,22 to an invention non-elected with traverse in the oral reply on 1/20/2006 as noted above, Applicant's Representative agreed to authorize the Examiner to cancel the non-elected claims 1,3-4,6,20,22, as given in the Examiner's Amendment below (see attached interview summary).

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Examiner's Amendment

8. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided

by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Johnathan T. Kaplan (Reg. No. 38,935) on 2/8/2006.

The application has been amended as follows:

In the specification:

"Conv rsion" (page 8, line 31) has been replaced with --Conversion--.

"S t" (page 10, line 1) has been replaced with --Set--.

"Tabl" (page 15, line 1) has been replaced with --Table--.

"D scription" (page 15, line 1) has been replaced with --Description--.

In the abstract:

The abstract has been replaced with the following text so as to form a single paragraph as follows:

--Relates to automatic conversion of assumption constraints, used in circuit design verification, that model an environment for testing a DUT/DUV, where the assumptions specify sequential behavior. Such assumptions are converted, with the use of logic synthesis tools, into a gate-level representation. For formal verification, a verification output is constructed from the gate-level representation and DUT/DUV assertion-monitoring circuitry. A formal verifier seeks to prove the verification output cannot indicate a design error. For simulation verification, the gate-level representation is converted into a hybrid representation comprising pipelines and combinational constraints. During simulation, the pipelines hold state information necessary for a

solution, of the combinational constraints, to be in accord with the sequential assumption constraints. For certain sequential assumption constraints, the combinational constraints are insufficient to insure avoidance of deadend states. In a deadend state, an assumption is violated. A method is presented for augmenting the combinational constraints to avoid deadend states.--

In the claims:

As per **claims 1,3-4,6,20,22**, the claims have been canceled.

As per **claim 2**, "comprising" (line 3) has been replaced with --performing--.

As per **claim 7**, --(High-Level Hardware Description Language)-- has been inserted after "HLHDL" (line 4).

As per **claim 21**, "comprising" (line 3) has been replaced with --performing--.

Allowable Subject Matter

9. **Claims 2,5,7-19,21,23** are allowed.

10. The following is an examiner's statement of reasons for allowance:

As per **claims 2,5,7-19,21,23**, the independent claims 2,5,21,23, from which the respective claims depend, recite the electromagnetic waveform comprising the computer program/the method/computer program product, for performing simulation verification, comprising the inventive steps or processes comprising the combination of the conversion and converting steps/processes as claimed, which correspond to Applicant's specification, page 4, line 27 to page 47, line 2. In particular, the prior arts made of record teach various methods/systems for circuit verification involving the use of logic synthesis involving various constraints (see **Rajan**, U.S. Application Publication

No. 2002/0055829, especially paragraphs [0019], [0027]-[0028]; **Moon et al.**, U.S. Patent Application Publication No. 2003/0121013, especially paragraphs [0010], [0035], [0040], [0116], [0131]-[0135]; **Williams et al.**, U.S. Patent Application Publication No. 2003/0191869, especially paragraphs [0177], [0203], [0280]; **Barzilai et al.**, U.S. Patent No. 4,763,289, especially col. 6, lines 5-65; **Ashar et al.**, U.S. Patent No. 6,163,876, especially col. 4, lines 28-64; **Basto et al.**, U.S. Patent No. 6,341,361, especially col. 3, line 55 to col. 4, line 7; **Ozaki**, U.S. Patent No. 6,389,580, especially col. 7, line 40 to col. 8, line 17; **Hsieh et al.**, "Synchronous Approach to the Functional Equivalence of Embedded System Implementations", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 8, August 2001, pp. 1016-1033, especially section III). However, none of the prior arts made of record teach or suggest the inventive steps/processes as claimed. Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

Conclusion

11. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Thursday, 6:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

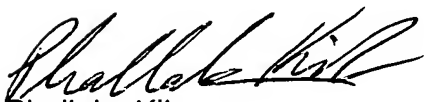
Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

571-273-8300



Phallaka Kik
U.S. Patent Examiner
February 8, 2006